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10/668,358	09/24/2003	Tetsuya Tanaka	2003_1313A	4687

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WENDEROTH, LIND & PONACK, L.L.P.
2033 K STREET N. W.
SUITE 800
WASHINGTON, DC 20006-1021

EXAMINER	
FENNEMA, ROBERT E	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/21/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/668,358	TANAKA ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *10-17,56 and 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *10-17 and 56-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *8/15/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 10-17 and 56-57 are pending. Claims 10-11, 13-14, and 16 have been amended as per Applicant's request. Claims 56 and 57 added as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 10-12 and 56 are rejected under 35 U.S.C. 102(b) as being anticipated by Patterson et al. (herein Patterson).

4. As per Claim 10, Patterson teaches: A SIMD processor for executing SIMD instructions, the SIMD processor comprising:

a first register operable to store data (Page B-7, V1-V3 are registers operable to store data);

a second register operable to store data (Page B-7, V1-V3 are registers operable to store data);

a flag storage unit operable to store a first flag (Page 130, the IR, a key part of any processing system);

a decoding unit operable to decode an instruction (Page 127, a decoder is necessary in all processing systems to allow instructions to be interpreted); and

an execution unit operable to execute the instruction based on a result of the decoding performed by the decoding unit (B-5, the vector functional units),

wherein the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying the first register and the second register (B-7, Figure B-3, for example ADDV), refers to the first flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the first flag stored in the flag storage unit indicates a first status (B-7, Figure B-3, with the flag being the second register operand. When the first and second register operands specify the same register (for example, V2 and V2), then the SIMD operation will only be executed on the operand held in the first register, as it will only be operating on the register which was specified in the first operand, since it was told to operate on itself), and (ii) on the operands held in the first register and the second register when the first flag indicates a second status (B-7, Figure B-3. When the second operand register is any register but the one specified in the first operand register, such as V3 as shown in the table, then it would in fact operate on both the first and second register).

5. As per Claim 11, Patterson teaches: The SIMD processor according to claim 10, wherein the SIMD operation is addition (B-7, Figure B.3, ADDV), and

wherein the execution unit adds (i) a value held in the first register and said value held in the first register when the first flag indicates the first status (B-7, Figure B-3, with the flag being the second register operand. When the first and second register operands specify the same register (for example, V2 and V2), then the SIMD operation will only be executed on the operand held in the first register, as it will only be operating on the register which was specified in the first operand, since it was told to operate on itself), and (ii) the value held in the first register and a value held in the second register when the first flag indicates the second status (B-7, Figure B-3. When the second operand register is any register but the one specified in the first operand register, such as V3 as shown in the table, then it would in fact operate on both the first and second register).

6. As per Claim 12, Patterson teaches: The SIMD processor according to claim 11, wherein the execution unit, when two pieces of data a1 and a2 are stored in the first register and two pieces of data b1 and b2 are stored in the second register, calculates (i) (a1+a1) and (a2+a2) when the first flag indicates the first status, and (ii) (a1+b1) and (a2+b2) when the first flag indicates the second status (B-7, Figure B.3).

7. As per Claim 56, Patterson teaches: The SIMD processor according to claim 10, wherein the first status of the first flag is either "0" or "1" (The register identifier could be a 0 or 1 corresponding with the other register in specific cases).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 13-17 and 57 are rejected under 35 U.S.C. 103(a) as being unpatentable over Patterson, in view of Probin et al. (herein Probin).

10. As per Claim 13, Patterson teaches: A SIMD processor for executing SIMD instructions, the SIMD processor comprising:

a first register operable to store data (Page B-7, V1-V3 are registers operable to store data);

a second register operable to store data (Page B-7, V1-V3 are registers operable to store data);

a flag storage unit operable to store a flag (Page 130, the IR, a key part of any processing system);

a decoding unit operable to decode an instruction (Page 127, a decoder is necessary in all processing systems to allow instructions to be interpreted); and

an execution unit operable to execute the instruction based on a result of the decoding performed by the decoding unit (B-5, the vector functional units),

wherein the execution unit, when the decoding unit decodes an instruction for performing a SIMD operation, the instruction including operands specifying the first

register and the second register (B-7, Figure B-3, any of the arithmetic operations), refers to the flag stored in the flag storage unit, and performs the SIMD operation (i) only on the operand held in the first register when the flag stored in the flag storage unit indicates a first status (B-7, Figure B-3, with the flag being the second register operand. When the first and second register operands specify the same register (for example, V2 and V2), then the SIMD operation will only be executed on the operand held in the first register, as it will only be operating on the register which was specified in the first operand, since it was told to operate on itself), and (ii) on the operands held in the first register and the second register when the flag indicates a second status (B-7, Figure B-3. When the second operand register is any register but the one specified in the first operand register, such as V3 as shown in the table, then it would in fact operate on both the first and second register), but fails to teach:

rounding the results of the operation.

Patterson teaches a processor which can execute vector processing instructions, but does not specifically teach an instruction which can round the operation result. However, Probin teaches several instructions which round, namely the vector average instructions (Page 10, these instructions add 1 to the result, which makes the additions round up. As an example, see two different results of an addition, 0010 and 0011 (2 and 3), an even and odd number, which when divided by 2 in binary, produce values of 1 and 1 (0001). By adding 1 to the results (0011 and 0100), the division by 2 is instead 1 and 2 respectively (0001 and 0010), thus rounding odd numbers up, while leaving even results the same). Probin teaches these instructions which are intended for a PowerPC

architecture, however, Patterson teaches that his example DLX architecture is incredibly similar and compatible with the PowerPC (C-1). Given that Patterson's basic architecture is compatible or at least similar to the PowerPC, it would have motivated one of ordinary skill in the art at the time the invention was made to use PowerPC instructions such as those that round (which would have been specified by an opcode (the second flag)), in order to take advantage of being able to use the PowerPC instruction set architecture.

11. As per Claim 14, Probin teaches: The SIMD processor according to claim 13, wherein the SIMD operation is addition (Page 10, addition is performed first in the average instruction), and

wherein the execution unit adds (i) a value held in the first register and said value held in the first register (Page 10, the vavgub instruction for example), when the two register operands point to the same register), and adds 1 to an addition result when the flag indicates the first status (Page 10, the average instruction adds a 1 to the result of the add), and (ii) the value held in the first register and a value held in the second register (Page 10, the vavgub instruction for example, when the register operands point to different registers), and adds 1 to an addition result when the flag indicates the second status (Page 10, the average instruction adds a 1 to the result of the add).

12. As per Claim 15, Probin teaches: The SIMD processor according to claim 14,

wherein the execution unit, when two pieces of data a1 and a2 are stored in the first register and two pieces of data b1 and b2 are stored in the second register (Page 1, vector registers hold multiple pieces of data in each register), calculates (i) (a1+a1+1) and (a2+a2+1) when the flag indicates the first status (Page 10, when the register operands are the same), and (ii) (a1+b1+1) and (a2+b2+1) when the flag indicates the second status (Page 10, when the register operands are not the same).

13. As per Claim 16, Patterson teaches: The SIMD processor according to one of claim 10,

wherein the flag storage unit further stores a second flag (Page 127, the IR also holds the opcode, which is a flag), but fails to teach:

wherein the execution unit determines whether to round the operation result or not depending on a value of the second flag.

Patterson teaches a processor which can execute vector processing instructions, but does not specifically teach an instruction which can round the operation result depending on a flag. However, Probin teaches several instructions which round, namely the vector average instructions (Page 10, these instructions add 1 to the result, which makes the additions round up. As an example, see two different results of an addition, 0010 and 0011 (2 and 3), an even and odd number, which when divided by 2 in binary, produce values of 1 and 1 (0001). By adding 1 to the results (0011 and 0100), the division by 2 is instead 1 and 2 respectively (0001 and 0010), thus rounding odd numbers up, while leaving even results the same). Probin teaches these instructions

which are intended for a PowerPC architecture, however, Patterson teaches that his example DLX architecture is incredibly similar and compatible with the PowerPC (C-1). Given that Patterson's basic architecture is compatible or at least similar to the PowerPC, it would have motivated one of ordinary skill in the art at the time the invention was made to use PowerPC instructions such as those that round (which would have been specified by an opcode (the second flag)), in order to take advantage of being able to use the PowerPC instruction set architecture.

14. As per Claim 17, Patterson teaches the SIMD processor according to claim 11, but fails to teach:

wherein the execution unit further divides the operation result by 2.

Patterson teaches a processor which can execute vector processing instructions, but does not specifically teach an instruction which further divides an addition operation result by 2. However, Probin teaches an instruction which divides an addition result by 2, in order to find the average of the two added numbers (Page 10). Given that the PowerPC architecture which Probin runs on is so similar to Patterson's example basic architecture, one of ordinary skill in the art at the time the invention was made would have been motivated to make use of PowerPC instructions such as an average instruction, either on a PowerPC of a design similar to Patterson's, or to make use of similar instructions on the DLX.

15. As per Claim 57, Patterson teaches: The SIMD processor according to claim 13, wherein the first status of the flag is either "0" or "1" (The register identifier could be a 0 or 1 corresponding with the other register in specific cases).

Response to Arguments

16. Applicant's arguments, see Page 16, filed 10/17/2006, with respect to the Objections to the specification have been fully considered and are persuasive. The objection of the specification has been withdrawn.

17. Applicant has essentially argued for both Claims 10 and 13 that Patterson fails to teach performing the operation on the operand held in the first register when a flag is a certain status, and on both the operand held in the first and second registers when the flag is a second status, when the two registers are both different. However, the current claim language does not explicitly require this limitation. Although two registers operable to store data have been claimed, with both registers being referred to by an instruction, the registers are not currently required to be different registers, and the fact that two registers were listed in the claim does not explicitly indicate that they are separate entities.

Conclusion

18. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:45-6:15.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Robert E Fennema
Examiner
Art Unit 2183

RF

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100